Report of the STT Review Committee

March 27, 2000

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The Committee was impressed with the general state of the STT project and the amount of progress made within the past few months. The Committee thanks the members of the STT group for their preparation for, and their cooperation with, the review process.

The remainder of this report is organized into three parts:

Part A: General findings and recommendations
Part B: Answers to the specific questions posed to the Committee
Part C: Further recommendations

A. General Findings and Recommendations:

The Committee did not find any reason for concern with the proposed algorithms, the general system design, nor the data flow and rates for the system. The Committee endorses the overall design, including the use of a local CPU for initialization, monitoring, and downloading (but see remarks below).

We are concerned, however, with the general schedule, and are not convinced that there will be a working STT by February 2002.

Hardware:

We are worried by the fact that design work on the motherboard will not start until April 2000. The three large daughter boards need a working motherboard for testing and debugging, and without it, all detailed development work will halt. (See also point **B.4** below.)

Software:

Although much of the STT is comprised of hardware, it still requires a large amount of software. This is particularly true for the initializing and monitoring CPU in slot 1. The STT group would clearly benefit from the addition of personnel in this area. We also encourage the STT group to consult with experts from Silicon and from L2 to borrow as much software as possible. (See also point **B.7** below.)

Testing:

System tests are likely to take more time than currently allocated. To meet the installation date may require a reduction in time allocated to the second prototype stage. Much of the test hardware will have to come from or be very similar to the silicon 10% test. If possible, the STT group should find additional personnel, who should learn to operate the 10% test stand, and then proceed directly with the integration tests.

B. Answers to the Specific Questions Posed to the Committee:

1) Timing and system flexibility:

We think that the STT system will meet L2 timing requirements. The Committee also believes that the design of the system will be sufficiently flexible, and will have enough built-in margin, to deal with the uncertainties of the expected system load.
Detailed recommendations: We recommend that the STT group remove the limitation on the allowed number of slots of the (VRB/VRBC) communication bus on the J3 back plane, in order to maximize hardware flexibility. Given that the existing engineering will be fully occupied, a possible approach would be to ask ESE to modify the SVX-VRB back plane.

2) Integration and data loads:

In order to judge the integration with L1, L2 and L3, the Committee recommends that the STT group put more effort into documentation. This should also help with the completion of the design of the PC boards.
Detailed recommendations: The interfaces between the STT and other D0 systems have not been specified clearly enough. Examples are the monitoring, the L2 Cypress to MBT connection, integrating the VBD, and the SCL interface (including resets). The protocol for VME (pre-) arbitration by the FRC, and the SCL_INITIALIZE procedure should be developed more fully. Continued interaction with the relevant experts is strongly encouraged.

The STT group should decide how many tracks to implement for their system - 32 or 46 tracks? The choice may impact STT performance at high luminosity with multiple minimum bias interactions.

The proposed data loads and event rates seem to be appropriate and well matched, both within the system, and in communication with the rest of the D0 trigger and DAQ system. In particular, the L2 protocol and physical implementation is well specified. Communication between the parties involved (the STT and L2 groups) is good. However, this area needs better documentation.

3) Readiness for Prototyping:

As stated by the STT group, the design is not yet at the stage where it can move to layout, prototyping and production. The Committee recommends internal design reviews before

layout begins. At the minimum there should be one person designated who reads all the documentation and verifies that the documents are mutually consistent.

4) Schedule:

The schedule, as presented to the Committee, is aggressive. It is unclear to what extent the schedule has already slipped. When funding was announced, the intent was to review the "final design" in December, while, in practice, a final design was not available even at the end of February. The group is encouraged to maintain a WBS budget and a schedule, with milestones reported through the normal management structures.

5) Beam-Spot Monitoring, Accelerator Interface, Monitoring in general:

Beam-spot monitoring and feedback to the accelerator seem to be understood. Issues and tasks related to downloading of run-dependent constants, and bookkeeping of position constants, tracking matrices, etc., are shared with the rest of D0. It is believed that the STT will be able to profit from developments and experience gained at the start of Run II, i.e., before the STT becomes operational.

Monitoring in general appears not to be sufficiently defined. The STT group should develop a plan for monitoring as soon as possible. Critical issues include whether the hardware adequately supports the monitoring and diagnosis of data-flow hang-ups and bottlenecks: should there be a slow clock for sampling histograms on the motherboard, for example? Some cards specify monitoring that is cleared on every read; others are cleared only on explicit command, making the monitoring software in the CPU unnecessarily complex.

6) Installation and Commissioning:

Test and installation plans should be pursued further, both in order to have better coordination with the overall schedule, and to ensure that adequate test equipment and facilities are available. The commissioning plans need to be fleshed out in enough detail so that any additional hardware requirements can be realized sufficiently early. In particular, the Committee feels that additional hardware, similar to the silicon 10% test, will be required for system testing of the STT (injection of G-link test signals). The Committee recommends that the STT group develop expertise with this hardware as soon as possible. Plans for using the hardware at Fermilab or at participating institutions should then be worked out in detail.

The STT group should reconsider the scope, timing, and location of the integration tests. The current schedule has the integration tests performed on an extremely aggressive timescale, just as the D0 experiment is rolling in. This may lead to problems of support at FNAL.

7) Personnel, schedule and budget:

Personnel:

The Committee agrees that the STT project would benefit from the addition of more personnel, in particular for the crate-embedded CPU, and in the areas of monitoring software, maintenance of the parameter database, and bookkeeping.

Schedule and Budget:

As boards progress to the selection of parts and layout phase, a detailed bottom-up budget should be worked out. A schedule risk can translate into a budget risk as far as engineering and technicians' salaries are concerned, and this must be considered in the overall analysis.

C. Further Recommendations:

Hardware:

The STT group is encouraged to consider whether using a single clock, 53MHz for the G-link and 53/2 for PCI, would meet throughput requirements.

The use of VIPA geographical addressing, to partition VME address space and to define PCI base addresses for initialization, is encouraged.

The Committee recommends that the STT group start work on specification and development of the (initialization, download, monitoring and readout) system in slot 1. If the STT group is going to piggyback off the work of the VRBC group, they should start consulting with that group soon. This is especially important given the requirements that will be placed on the CPU for providing a private DAQ for system and commissioning tests.

Given the difficulties experienced by other systems in this area, the STT group is encouraged to strive for an early implementation and test of the L3 readout connection.

Simulation:

Alignment effects and the effects of beam movement should be studied.

The effects of barrel offsets on the constant term in resolution, on the trigger rate and on the TFC lookup memory seem to warrant further study.

Simulation studies should include the proper number of minimum bias events overlaid.

The STT group should determine the TFC time budget by varying the processing time and measuring deadtime.

The STT queuing simulation should include current models of timing parameters and, particularly, any sources of timing fluctuations that generate long tails in time required. The queuing model should be integrated with an overall model of Level 2 in particular, as well as with the overall D0 DAQ model.

The trigger simulation should be fully integrated with the emulation being developed, in accordance with the guidelines being developed by the Trigger Emulation Design Group. Interaction with the L2 group may help in sidestepping some of the current technical problems.

Software:

The STT group should come up with a plan for testing/commissioning new TFC algorithms while data is being taken. It appears that the TFC algorithm will change more frequently than other elements. It should be checked whether the STT can fit into the L2 data-shadowing plan, with fan-out of all the necessary inputs to a shadow crate, or whether shadow TFC's can be integrated into STT crates. Ideally, there should be a test stand setup where all algorithms can be tested.